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EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/074,061	SOLTIS ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 11-17* is/are pending in the application.

4a) Of the above claim(s) *9 and 10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8, 11,12, 13-16,17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-8,11-17 are presented for examination. Claims 9,10 have been canceled.

2. Applicant's arguments with respect to claims 1-8, 11-17 have been considered but are moot in view of the new ground(s) of rejection. However, this action also includes examiner's response to applicant's remarks in order to clarify some issues. In the remarks, applicant argued that :

a) Fetterman did not disclose hazard detection and did not disclose one-to many register aliasing;

b) Panwar did not disclose reducing the complexity of hazard logic through use of aliasing;

c) neither Wan nor Panwar disclosed a register file groped into two or more non-overlapping equally sized stacks of consecutive registers.

3. As to a) Fetterman clear aught hazard detection (see the determination; of the validity of the speculative result of the corresponding architectural register to the committed real register in col.8, lines 45- 49). As to the one to many register aliasing ,

see one of the (EAX) HEDN registers in fig.3 in the aliasing table to two or more registers (see EAX register mapping to corresponding physical register and real register in a single entry of EAX in col.8, lines 41-49) .

4. As to b) , Panwar taught to reduces the resource required for performing the dependency tracking (see col.4, lines 45-53). Therefore, Panwar was directed to reducing the complexity of the hazard detection logic. As for aliasing, see aliasing in the background in col.2, lines 42-57).

5. As to c), see newly cited Kumar et al. (5,513,363) in this action below.

6. Based on recent Interim 101 Guidelines and the group training on 02/22/06, this action also included "101" rejection . Therefore, it is a non-final action in order to allow applicant a chance to respond.

7. Claim 4-6 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the relationship between the processing of the instructions and the writing the bypass data.

8. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted elements are: the relation between the data hazard detect logic (preamble) and the common data hazard detection logic (claim 7, lines 4-5).

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

9. Claims 1,4, 7, 13, 15,16 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

10. As to claim 1 , is read as a non-statutory process. The preamble recites a "processor". However, the claim body does not reflect the structural elements of the processor to support the processor. The steps of identifying, aliasing, and detecting are read as programming steps taken to achieve a particular result, not the final result achieved by the steps with is useful, tangible and concrete. It is not useful because there is no final result, thus no real word value . It is not tangible because there is no

structural element relation of the processor to support the processor found in the claim . The claim recite "stack register" . However, the relation of the stack register with the processor is not clear. It is not concrete because it is unpredictable. The "wherein" clause suggests optional and does not require the steps to be performed, and does not limit the scope of the claim .

11. As to claim 7, claim 7 is directed to "..data hazards detect logic for..." The language " logic" raised a doubt as whether applicant is seeking protection of the an abstract idea. No physical transformation can be found in the claim. The aliases of the row –to row register file for non-consecutive rows of the register file is read as relationship of the data sets. Therefore, it is potentially a data structure per se without a computer readable storage medium stored therein the hazards detection logic. Claim 7 also recite "... of a processor...", but it is read as the logic taken to achieve a particular result, not the final result achieved by the logic. Therefore, no substantial practical application can be found.

12. As to claims 15,16, both claims 15,16 recites "hazard detection logic". It is not sure whether applicant is seeking the protection of an abstract idea. Suggestion : "hazard detection logic circuit", or the like might help to clarify the language.

13. As to claim 13, claim 13 recites "data hazard logic dependency..", The logic dependency is also an abstract idea. Suggestions : "... reducing data hazard dependency in a data hazard logic circuit....on size of a register file within a processor..."

14. As to claim 4, claim4 could appear to read as a data structure per se, The register file of two or more non-overlap equally sized stacks of consecutive registers could be a mapped tree structure of two non-overlapping branches which is noting more than a data structure, and the hazards detection logic, which raised a doubt as whether applicant is seeking protection of the an abstract idea, could be a logic relationship, therefore, not tangible. Although claim 4, recites "execution unit having an array of pipelines for processing insertions", it does not reflect functional relation between other elements of the claim to permit the function to be realized (see 112 above). Preamble recites "program instructions", but no computer readable storage storing the program instructions could be found in the claim. As to the "processor" in the preamble , no structural elements of the processor in the claim body to support the "processor" can be found.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 8, 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fetterman et al. (5,627,985) in view of Kumar et al. (5,513,363).

16. As to claims 8,15, Fetterman taught :

a) aliasing each register identifier of a group of register identifiers (see one of the (EAX) HEDN registers in fig.3 in the aliasing table) to two or more registers (see EAX register mapping to corresponding physical register and real register in a single entry of EAX in col.8, lines 41-49) of a register file of the processor; and

b) determining data hazards with the register file by processing one or more of the register identifiers (see the determination; of the validity of the speculative result of the corresponding architectural register to the committed real register in col.8, lines 45-49).

17. The architectural registers are the EAX-EDX (see col.7, lines 10-15). Fetterman did not specifically teach the non-overlapping groups of consecutive registers as claimed. However, Kumar taught a scalable register file which was divided in two subsets of equal size (see the two subsets in col.3, lines 1-13, see also col.7, lines 31-41). It would have been obvious to one of ordinary skill in the art to use Kumar in Fetterman for including non-overlapping registers file groups consecutive registers as clamed because the use of Kumar could provide Fetterman the ability to provide a register file adapted to the specific number of processing units required in the system, therefore, minimizing the access time due to the hardware size of the registers, and it could be achieved by predefining the scalable register file of Kumar into the configuration file of Fetterman with modified control parameters (e.g. the register size and register number) so the particular size of the Kumar's register file could be

recognized by Fetterman , and because Fetterman was seeking to minimize the complexity of managing the speculative and committed status of the register files, and Kumar was also working toward the efficiency of the access to of the register file, one of ordinary skill in the art should be able recognize the advantage of the scalable register file in Kumar could reduce the complexity of managing the register files of Fetterman, and therefore, provided a solution to Fetterman, and in doing so, provide a motivation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al. (5,826,055) in view of Panwar (5,884,070) in view of Kumar et al. (5,513,363).

19. As to claim 4, Wang disclosed at least :

a) register file (see register file col.10, lines 1-5);

b) an execution unit having an array of pipelines for processing instructions (see col.l ,lines 45 52) and for writing bypass data in to the register file (see col.10, lines 1-5),

c) data hazard detection logic for detecting data hazard detection (see col.l, lines 54- 54 for background, see col.6, lines 57-67).

20. Wang did not specifically show the aliasing for two or more rows of the register files as claimed. However, Panwar disclosed aliasing of two or more rows in a register file (see fig.1B). See the aliased register f4 and register f5 with f4 ID in fig. See fig.IA for rows of original register file. It would have been obvious to one of ordinary skill in the art to use Panwar in Wang for including the aliasing of the two rows as claimed because the use of Panwar could provide the capability of Wang to accept different groups of registers in a given reference, therefore reducing the hardware space, and it could be achieved by predefining the aliased register file of Panwar into Wang with modified register pointer so that the aliased rows of register file of Panwar could be recognized by Wang in order to archive the reduced dependencies control of Wang , and because Wang also suggested the use of aliased register table as background (see page 2 , lines 7-9 of cited reference in Wang), and for the above reasons, provided a motivation.

21. Neither Wang nor Panwar specifically show the non-overlapping equal size of the register file groups as claimed. However, Kumar taught a scalable register file which was divided in two subsets of equal size (see the two subsets in col.3, lines 1-13, see also col.7, lines 31-41). It would have been obvious to one of ordinary skill in the art to use Kumar in Wang for including non-overlapping registers file groups consecutive registers as clamed because the use of Kumar could provide Wang the control capability to adjust to a predefined set of number of processing units with divided or smaller groups of register files, thereby reducing the latency of the read/write cycles and it could be done configuring the scalable register file o of Kumar into the Wang

with modified register length so the specific length of Kumar's register file could be recognized by Wang , and because Wang also taught that each of his register file (see register array 404) had its own dedicated address (see col.12, lines 17-20), which was a suggestion of the applicability of non-overlapping register files , for example, each address line of the register file was unique , therefore, no overlap, and for the above reason, provided a motivation.

22. As to claim 5, Wang also included a register ID file (see the TAG generated by RRC 204 in col.9, lines 9- 46, see the RRC 204 for facilitating the hazard detection in col.7, lines 5-24).

23. Claims 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iadonato et al. (5,371,684) in view of Clift (6,598,149) in view of Lai (5,416,749) .

24. As to claim 7, Iadonato also included at least :

a) a register file (1 17 register file) (see Fig.II);

b) register ID file (it is ID file because compared the addresses of the registers) for providing hazard detections (see fig.2 108) by common detection logic (see how the conflict of the source and destination registers being detected in col.6, lines 63-68, col.7, lines 1-20) .

25. Iadonato did not disclose the row to row hazard detection as claimed. Iadonato disclosed register hazard detection in row to column format (see figs. 2). However, Clift disclosed a system including register file (10) of R0-R7 architectural registers, each of

the RO-R7 occupied one row in the register file (10) (see fig.1). It would have been obvious to one of ordinary skill in the art to use Clift in Iadonato for including the row to row detection as claimed because the use of Clift could provide the control ability of Iadonato to accept specific group of registers in rows in an integrated format, thereby eliminating the circuit overheads of the memory, and therefore, reducing the wait time caused by the hardware, and it could be done by configuring the register file of clift, which taught the architectural register were organized in rows, into Iadonato with modified read/write pod, such that the particular row of the register file of Clift could be recognized by Iadonato in order to enhance the hazard detection capability of Iadonato, and in doing so, provided a motivation.

26. Neither Iadonato nor Clif taught the non-consecutive rows as claimed. However, Lai taught a system including the non-consecutive rows (see odd row and even row in fig.2). It would have been obvious to one of ordinary skill in the art to use Lai in Iadonato for including the non-consecutive rows because the use of Lai could provide Iadonato the ability to in a specific pattern of rows, such as the even or odd rows, and it could be done by reconfiguring the odd and even rows of Lai into Iadonato such that the non-consecutive rows of Lai could be recognized by Iadonato, and because the examiner holds that non-consecutive rows were already known in the art , such as the one taught by Lai, and what would be obvious to one of skill in the art is a different question from what would be obvious to a layman. An artisan is likely to extract more than a layman from reading a reference. Here, Iadonato already taught the hazard detection between the row and column , and one of ordinary skill in the art should be

able to recognize the use of row to row, or row to column in any order. Clif is used to show row to row register file , and Lai is used to show row to row in a specific order, such as non-consecutive.

27. Claims 8,11,12, 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Panwar (5,884,070) in view of Kumar et al. (5,513,363) .

28. As to claim 8, Panwar taught :

a) aliasing each register identifier of a group of register identifiers to two or more registers (see the aliased registers in fig.1 B);

b) determining data hazard within the register file by presenting one or more register identifiers (see the determination of data dependencies in col.3, lines 39-67, col.4, lines 1 - 1 9).

29. Panwar also mapped non-overlapping registers (see f4 and f6 in fig .1 B) Panwar also included two more rows in hazard detection logic (see dependencies detection in col.l., lines 39-67, col.4, lines 1-19).

30. As to 11, see the fewer possible dependencies in col.8, lines 49-54, col.10, lines 34-37).

31. As to claims 12, 17, Panwar also taught 32 register identifiers (see fig.1A f0-f31).

32. Panwar did not specifically show the non-overlapping group so consecutive registers of equivalent size as claimed. However, Kumar taught a scalable register file which was divided in two subsets of equal size (see the two subsets in col.3, lines 1-13, see also col.7, lines 31-41). It would have been obvious to one of ordinary skill in the art to use Kumar in Panwar for including non-overlapping registers file groups consecutive registers as clamed because the use of Kumar could provide Panwar the ability to provide a register file adapted to the specific number of processing units required in the system, therefore, minimizing the access time based on the hardware size of the registers, and it could be achieved by predefining the scalable register file of Kumar into the Panwar with modified register length so the a predefined length of the Kumar's register file could be recognized by Panwar , and because Panwar also show a non-overlapping register file, though no equivalent size was shown, the number of registers could have suggested the use of any size, including the equivalent size, and for doing so, provided a motivation.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

33. Claim 15 is rejected under 35 U.S.C. 102(b) as being anticipated by Panwar (5,884,070).

34. As to claim 15, Panwar taught :

a) aliasing each register ID within hazard detection logic to tow or more registers of a register file (see fig.l B);

b) determining the data hazard by matching register ID within the detection (see the dependencies detection in col.3, lines 25-67, col .4, lines 1-19, col.8, lines 17-54).

35. As to the non-consecutive registers , see the even operand register id 0,2,4 in fig.1B.

36. Kumar (5,513,363) and Lai (5,416,749) are newly cited references. All other references were already cited on record.

37. Claims 13-14 are allowable, upon pending condition of the "101" above, over the art of record for ' selecting register file id size, aliasing at least one entry of the register ID file to two or more registers of the register file, each of the two or more registers being located in a non- overlapping group of sequential registers equivalent in size to the over selected resister ID file size; and evaluating matches between entries of the register ID file in the hazard logic without distinguishing between common aliased entries of the register file.

38. Claim 16 is allowable, upon pending condition of the "101" above, over the art or record for reciting a method of stack register aliasing in data hazard detection logic in a processor, comprising aliasing two or more non-overlap groups of consecutive registers of a stacked register file to one group of consecutive register IDs within the

data hazard detection logic each register ID aliasing one register from each group of consecutive resisters; and detecting data hazards, if any, associated with y first and second register of the stacked register file by comparing a first aliased register ID of the first register to a second aliased register ID of the second register within the data hazard detection logic.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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